Richard Brice's de-jittering circuit for digital audio can be inserted between a CD player and external d-to-a converter for improved fidelity, particularly at low frequencies. It also removes copy code and can be modified to convert between formats.

Improve your digital audio

Jitter on a digital audio signal is known to cause appreciable signal degradation. All the more irksome then, that its elimination is extremely difficult by means of classical PLL-style digital audio interface receivers. This is especially so when the modulation is at a relatively low frequency, such as that caused by power-supply induced coupling.

This article describes a practical circuit for a digital interface unit that may be used to remove low-frequency jitter from a digital audio signal. Its use between a CD output and an external converter is described.

The unit has a number of useful ancillary provisions that allow it to be modified to transcode between the SPDIF consumer interface and the various AES/EBU interfaces. It also strips copy-code, allowing direct digital copies to be made.

Table 1. Aperture effect – even when the sampling pulse width equals the sampling period, loss at the pass-band edge is only –3.9dB.

T_s/T_o	Attenuation at pass-band edge
1	3.9dB
0.5	0.9dB
0.25	0.2dB
0.2	0.1dB
0.1	0.04dB

Background

The quality of digital audio is mathematically definable in terms of; the sampling frequency employed, the bit 'depth', the sampling-pulse aperture and time uncertainty. Expressions for the first two are well known. The effect of the latter two parameters is less well appreciated.

Sampling pulse width (as a proportion of sampling period) simply has an effect on frequency response as defined in the expression,

$$20\log sinc\left(\frac{\pi}{2}\times\frac{f}{f_n}\times\frac{T_s}{T_o}\right)\text{dB}$$

where, T_s is the duration of the sampling pulse (aperture) and f_n is the Nyquist frequency limit. Note that *sinc* is shorthand for sin*x*/*x*. This is termed 'aperture effect' and is actually relatively benign.

As **Table 1** indicates, even when the sampling pulse width is equal to the sampling period, the loss, at the band edge, is only –3.9dB. Provided $T_s<0.2T_o$, the effect is pretty negligible.

In any case, frequency response 'droop' can always be made up in the design of the reconstruction filter following the d-to-a converter – where it is often referred to as sinx/x correction.

Why is jitter a problem?

The effect of sampling-pulse time uncertainty or 'jitter' is much more destructive. Because all signals change their amplitude with respect to time, the effect of a slightly misplaced sampling point has the effect of superimposing a distortion on the original waveform, effectively reducing available dynamic range.

This next equation defines the limit of sampling uncertainty, dT, for a digital system of n bits,

$$\frac{dT}{T_o} = \frac{1}{\left(\pi \times 2^{n-1}\right)}$$

Working through an example, a sixteen-bit audio system with 48kbit/s sampling must have a jitter performance of less than 200ps in order to preserve the theoretical dynamic range available from the 16-bit system. In other words the jitter must be just 0.001% of the sampling period!

Even if this requirement has been met in the recording stage, for absolute fidelity to be preserved, this value must be 'recreated' in any subsequent conversion to analogue for playback.

Phase-locked loop receivers

Most digital-audio converters rely on a phase-locked loop front-end to extract clock from the self-clocking AES/EBU or SPDIF digital-audio interface and to use this in the reconstruction of the analogue signal.

Several very good chips exist for this purpose, one of the most famous being the *CS8412* from Crystal Semiconductor. Should there be any high-frequency jitter on the interface, the PLL type receiver does a very good job in rejecting it. But, at low frequencies, it has no effect whatsoever, as **Fig. 1** shows.

This is unfortunate for the audiophile because jitter very often exists at much lower frequencies, usually due to the interaction of other analogue or digital signals or to power-supply induced effects.

Experiments have shown that the effect of substantially monotonic jitter indicates that the limits defined in the second equation still apply – even on modern over-sampling a-to-d and d-to-a converters.

Asynchronous sample-rate conversion

The construction of high-frequency phase-locked loops with low-frequency rejection is no mean task. Effectively the circuit must behave like a resonant circuit with a Q of thousands; a design constraint that usually compromises lock-time and centre frequency variability without recourse to complicated multi-stage designs.

Fortunately there exists an alternative, in the form of a family of chips from Analog Devices. These are based on asynchronous sample-rate conversion, or ASRC, technology.

There is more than one way to describe the nature of asynchronous sample rate conversion. The easiest to understand is the interpolation-decimation model in which the input signal is over-sampled to a much higher rate, digitally low-pass filtered and re-sampled at the output sample frequency.

Unfortunately, while easy to understand, the interpolation-decimation model is not a suitable basis for a practical system. This is because the output of such a system is only the

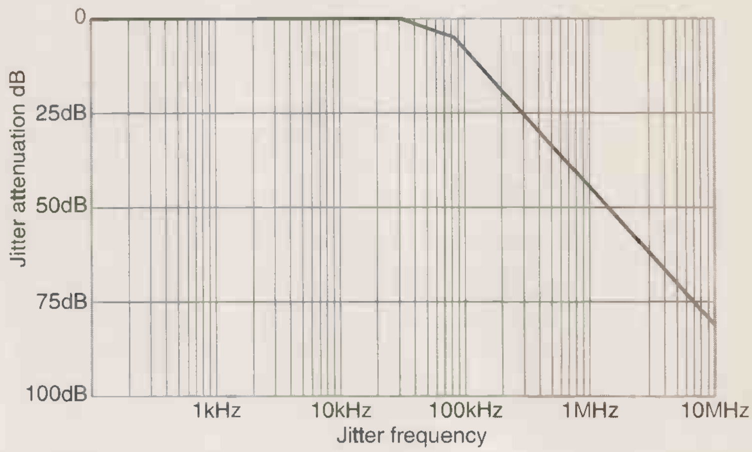


Fig. 1. Phase-locked loop receivers like the CS8412 do a very good job of removing jitter at high frequencies, but they do nothing for low frequency jitter.

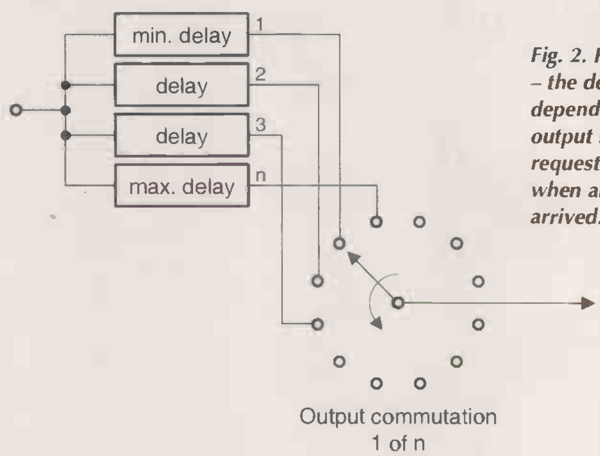


Fig. 2. Polyphase filtering – the delay chosen depends on when an output sample is requested in relation to when an input sample arrived.

nearest appropriate value in a temporal sense.

There is no theoretical reason why the interpolation shouldn't be carried out at a fast enough rate to make this viable. But there exist some very good practical reasons why it is not.

For instance, in order to achieve a reasonable performance – and this means, to achieve 16-bit levels of THD+N across the 0 to 20kHz audio band – the interpolation up-sample frequency would need to be over 3GHz! Clearly, this is an impracticable rate for a low-power IC, so the Analog Devices chips use a less commonly known method of sample-rate conversion called polyphase filtering.

Polyphase filtering

In the polyphase filter ASRC, the digital audio sample sequence is over-sampled – but at a manageable rate of megahertz. It is then applied to a digital FIR low-pass filter in which the required impulse response – 20kHz cut-off – is

Thinking of prototyping it?

For those interested in building the circuit, PCBs, are available. For more details contact Richard Brice via e-mail richard@perfect-pitch.demon.co.uk.

itself highly over-sampled.

The filter is 'over-sampled' in the sense that it comprises many times the required number of coefficient sample taps to satisfy the Nyquist criterion. This means that, at any given moment, only a sparsely sampled subset of coefficients of this filter need be chosen to process the input samples.

These subsets of coefficients, create a kind of 'sub-filter', each possessing an identical 0 to 20kHz magnitude response but with a fractionally different group delay – hence the term 'polyphase'.

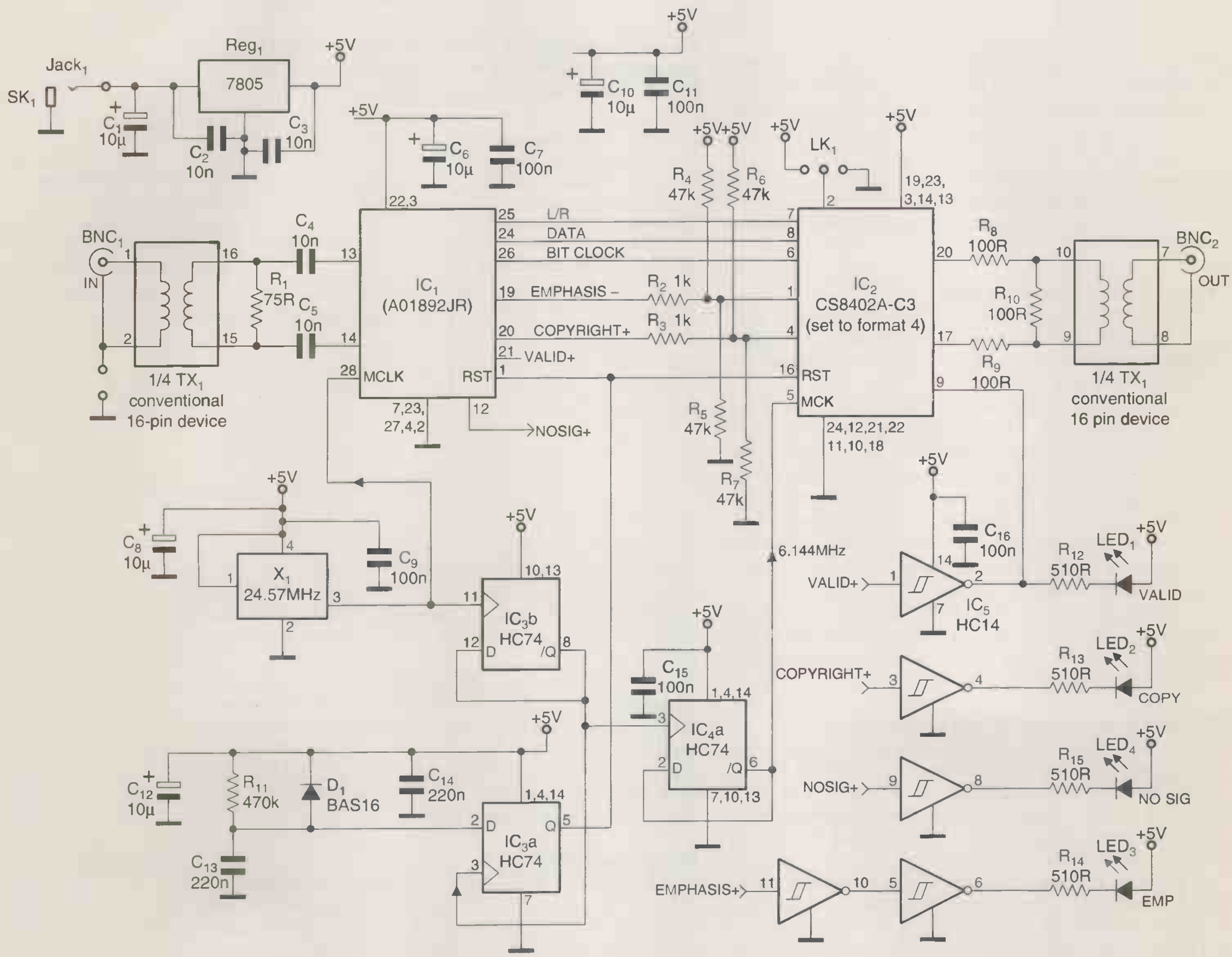
It is as if the input signal was being applied to a very great number – i.e. thousands – of digital delay-lines, each with a slightly differing delay. This is shown greatly simplified in **Fig. 2**.

The sample-rate conversion process works like this; if a request for an output sample occurs immediately after an input sample has arrived, a polyphase filter is chosen that imposes a short group delay. If a request for an output sample occurs late in the input-sample period, a polyphase filter that imposes a long group delay is chosen. In this fashion, the amplitude of the output sample is precisely computed at the desired output sample frequency.

Looking at the output commutator in Fig. 2, it's possible to imagine that, provided the relationship between the input and output frequencies is not completely random, there will be a pattern to the switch selection when looked at over a certain period of time.

Indeed, provided the input and output frequency are relatively stable, you can imagine the commutator revolving at the computed difference frequency between the input and output sample frequency.

This process is controlled, within the Analog Devices parts,



Note:
1 in PRO mode, EMP not indicated, flag **ALWAYS** set
2 in PRO mode output **ALWAYS** flagged stereophonic
3 consumer flags - 48k; COPY and EMP are transparent, so is validity

Fig. 3. Complete jitter remover for digital audio signals. It can be modified to transcode between SPDIF and various AES/EBU interfaces and it strips copy-code – allowing direct digital copies to be made.

by an on-chip, digital servo-control system that bases its commutation decisions not an instantaneous measurement, but rather on a digitally filtered ratio.

It is the effect of this powerful, low-pass filtering mechanism that greatly reduces any jitter that may be present on the sample clocks – even when the jitter frequency is just a few tens of hertz.

Implementing the design

Figure 3 is a practical implementation of the *AD1892* used as a jitter rejection device for use between the output of a CD player and the input of an outboard d-to-a converter. The *AD1892* is not just an ASRC. It is also an AES/SPDIF interface receiver too, so the circuit implementation is very simple.

The *1892* has some limitations, the most severe of which is that it only retains its performance over a limited range of upward sample-rate conversion and a very limited range of downward rate conversion.

For this design, I decided to use an up-conversion from 44.1kHz to 48kHz. The part works well at these two rates and the master oscillator – which must be 512 times output sample rate; 24.576MHz – is relatively easy to source at this frequency.

The SPDIF signal arrives at TX_1 – one part of a 16-pin, four transformer data-bus isolator – and is terminated, on the far side of the transformer by R_1. The signal is applied directly to the *1892* via coupling capacitors, C_4 and C_5.

The master output clock is derived from a small 24MHz crystal oscillator. Having been broken down into separate clocks and data by the Analog Devices part, the composite AES/SPDIF signal is put back together again by the Crystal Semiconductor *CS8402* transmitter chip. This too requires a master clock, but at one quarter of the frequency of the *AD1892*, hence the inclusion of the divide-by-two bistables IC_3 and IC_4.

SPDIF output is via transformer TX_1, which is another part of the same data-bus isolator used for the input. Note resistors $R_{8,9,10}$: these produce an output impedance of 75Ω at a level of about 2V. This is above that specified for SPDIF, which is 1V and is therefore a bit non-standard.

I made the choice for two reasons. Firstly, I have found that outboard d-to-a converters like to have a bit more level. Secondly, by changing the position of LK_1, the circuit may be used to encode a digital signal to the unbalanced form of the professional AES/EBU digital interface. This requires the higher output level.

Such provisions make the circuit useful if you need to interface a non-professional CD player in a digital studio. The output is also quite suitable for driving symmetrical a 110Ω AES-style interface, *mutatis mutandis*.

User indications

The circuit includes several user LEDs to indicate; validity, copy-code, pre-emphasis and signal loss. These are derived and decoded by the *AD1892*. The LEDs are driven by an HC14 and are primarily there for amusement since no user intervention is required.

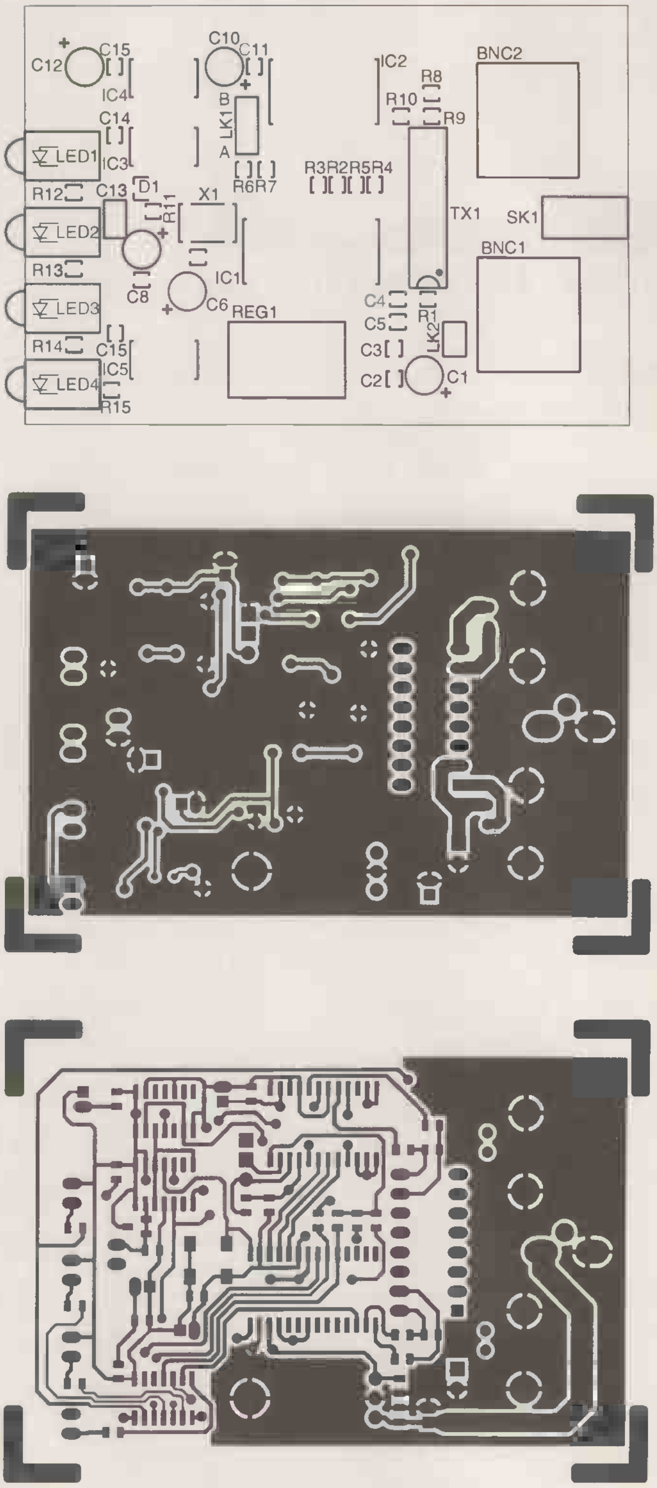
Emphasis state and Copyright prohibit are decoded and re-coded by the *CS8402*. Pull-up, pull-down resistor positions are provided here to allow for various options. The most useful of these is the removal of R_3 and R_6, which strips copy-code and allows direct digital copies to be made.

The layout of my prototype is shown in **Fig. 4**. Note the extensive use of ground-plane. Note that the signal inputs and outputs are on BNC as I prefer this connector enormously to the RCA phono alternative.

The power supply input is squeezed between the input and output and the whole circuit is enclosed in a little anodised, aluminium extrusion box, no bigger than a household box of matches. It is ideally suited for sitting on top of a CD player or d-to-a converter.

Although it's unwise to be adamant in this area, everyone who has listened to the circuit has been amazed by the improvement in quality that it yields; especially in definition at the bass-end of the spectrum. ■

Fig. 4. Layout of the author's prototype PCB.



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